DESIGN AND IMPLEMENTATION OF VLSI ARCHITECTURE ALGORITHMS FOR DIGITAL IMAGE WATERMARKING

A THESIS

Submitted by

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ABSTRACT

Nowadays, digital documents can be distributed through the World Wide Web to a large number of people in a cost-efficient way. The increasing importance of digital media, however, brings also new challenges as multimedia content is effortlessly duplicated and even manipulated. There is a strong need for security services in order to keep the distribution of digital multimedia work both profitable for the document owner and reliable for the customer. Applications of copy right information or watermarking techniques in the digital data transmission are must for ownership protection. Additional information (watermark) such as a symbol or a text can be added to the original image and this process is called watermarking, data embedding or information hiding.

Watermarking technology plays an important role in securing the business as it allows placing an imperceptible mark in the multimedia data to identify the legitimate owner. Security level offered by the watermarking techniques based on hardware is higher than the software based watermarking techniques. In hardware watermarking implementation, the data is untouched by an external party. Development of efficient watermarking mechanisms has become unavoidable. The purpose of this thesis is to investigate and implement the spatial and the frequency domain watermarking in Field Programmable Gate Array (FPGA) for still camera and biomedical images.

At first, an algorithm is developed for low power, high performance, real time, reliable and secure vector based One Dimensional

Discrete Cosine Transform (1D-DCT) watermarking technique to replace the existing Two Dimensional Discrete Cosine Transform (2D-DCT) watermarking system. This algorithm is designed to aim at reducing the computational complexity involving the scaling and embedding factors prominently used in any visible watermarking technique. To minimize distortion in the original image during the embedding process, edge block of an image should be least altered. It has been established that the computation of the scaling and embedding factors for each individual block is unnecessary when the allowed tolerance level in the result is not too stringent. The process is applied independently on each 1x8 vector as it can start as soon as it gets the first vector from the image and the watermark memory. Evaluation of this work is based on synthesis and timing report, which is obtained from ISE 10.1. To test the performance, the design is implemented on FPGA to analyze the resource utilization and throughput. The system has a high throughput of 8.06Gbits/s, which is high, when compared with other contemporary results of similar research. The system interleaving time is 5.293ns and it has 149 input and output pins.

In some applications, scaling and embedding factors are essential to employ differential watermarking based on block properties. In order to have a better block level control over the selection of scaling and embedding factor, a novel algorithm based on block level is developed. Minimal visual perception analysis scheme has been used to select different values for each block to be watermarked. Conventional 1D-DCT requires 64 multipliers and adders. Here, fast 1D-DCT is introduced for watermarking process to

minimize the resource utilization. In addition to fast 1D-DCT, a new mathematical model is developed to reduce the computational complexity for the calculation of embedding and scaling factors. Throughput achieved based on this Very Large Scale Integrated (VLSI) architecture is 5.21Gbits/s with a total resource utilization of 4058BELs. The system processing time is 4.32ns and it has 146 input and output pins.

To make use of spatial and frequency domain features, a combined pixel and vector based visible watermarking technique is introduced. In this approach, the user has to choose the watermark to be embedded, on the basis of which, watermarking process is done either as a pixel by pixel operation under spatial domain or as a vector form of operation in frequency domains. Clock gating technique is employed to reduce the power by preventing unnecessary switching in a path. The architecture data path consists of a nine stage pipeline capable of watermarking on pixel based operation and a seven stage pipeline capable of watermarking on vector based operation. The dual image watermarking architecture datapath consists of a thirteen stage pipeline. The throughput achieved is 8.6Gbits/s with a total area utilization of 7512BELs. A study was also undertaken about the throughput achieved by hardware and the same was compared with the existing hardware implementations.

Invisible watermarks have an advantage over the visible watermarks. Discrete Cosine Transform (DCT) watermarking techniques are weak against geometric attacks like rotation, scaling, cropping, etc. In order to strengthen the original image before the process of DCT to restrict the attacks,

we developed a technique for irreversible watermarking approach robust to affine transform attacks. The technique applied here is moment based normalization, which is invariant to affine transform attacks. Simulation and experimental numerical values such as performance, robustness, image quality and detector response are obtained by using the image processing tool in MATLAB 7.6. A single efficient algorithm for invisible watermarking was tested with different types of images to check its feasibility for images of various fields. Test results prove that the algorithm is suitable for biomedical, still camera image and satellite images. This would help in designing hardware for the tested algorithm to make a single chip for multiple types of images.

In our proposed hardware and software watermarking technique, hardware process time is very less than the software processing time. The future works may concentrate on the implementations of video watermarking technique. This type of watermarking provides a means of forensic analysis for combating media piracy. Future works can also concentrate on the implementation of the design in the form of chip using Application Specific Integrated Circuit (ASIC) to reduce the power.

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